

Notice of References Cited		Application/Control No. 09/840,500	Applicant(s)/Patent Under Reexamination TSAI, ROGER S.	
		Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,128,768	10-2000	Ho, William Wai Yan	716/5
	B	US-5,966,520	10-1999	Buer et al.	716/6
	C	US-6,133,132	10-2000	Toprac et al.	438/595
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Muller et al., Device Electronics For Integrated Circuits 2 nd Edition 1986. pg. 475-516.
	V	Biswas-B ., "Modeling and Simulation of High Speed Interconnects" Dissertation-- University of North Carolina State. 1998. pg. 1-67.
	W	VTT Electronics. "Research Activities in Microelectronics 2000" 2000. pg. 1-71.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.